UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	990531	Total Pages	

First Named Inventor or Application Identifier

Hidefumi OKADA

Express Mail Label No.

jc408 U.S. PTO 05/26/99

Check Box, if applicable [ ] Duplicate

APPLICATION ELEMENTS FOR:

DIGITAL CAMERA

ADDRESS TO: Assistant Commissioner for Patents
BOX PATENT APPLICATIONS
Washington, D.C. 20231

jc549 U.S. PTO 09/318614 05/26/99

1. [XX] Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)

2. [XX] Specification Total Pages [21]

3. [XX] Drawing(s) (35 USC 113) Total Sheets [8]

4. [XX] Oath or Declaration Total Pages [2]

a. [XX] Newly executed (original)

b. [ ] Copy from prior application (37 CFR 1.63(d)
(for continuation/divisional with Box 17 completed).

i. [ ] Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation by reference (useable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [XX] Power of Attorney

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	990531
	First Named Inventor or Application Identifier	
	Hidefumi OKADA	
	PAGE 2 OF 3	

10. [ ] English translation Document (if applicable)

11. [ ] Information Disclosure Statement [ ] Copies of IDS Citations

12. [XX] Preliminary Amendment

13. [XX] Return Receipt Postcard (MPEP 503)

14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired.

15. [XX] Claim for Convention Priority [1] Certified copy of Priority Document(s)

a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119. The certified copies/copy have/has been filed in prior application Serial No. _____.
(For Continuing Applications, if applicable).

16. [ ] Other _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

[ ] Continuation [ ] Division [ ] Continuation-in-part (CIP) of prior application no. _____/_____

FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic Fee $760.00
Total Claims	24 - 20	4	x $18.00	72.00
Independent Claims	2 - 3		x $78.00	
Multiple Dependent Claims			$260.00	
			Basic Filing Fee	832.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			$40.00	40.00
TOTAL				$872.00

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	990531
	First Named Inventor or Application Identifier	
	Hidefumi OKADA	
	PAGE 3 OF 3	

[XX] A check in the amount of $872.00 is enclosed to cover the filing fee of $832.00 and the assignment recordation fee of $40.00.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of _____ to cover the filing fee and the _____ assignment recordation fee. A duplicate of this sheet is attached.

[XX] The Commissioner is hereby authorized to charge payment for any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. **01-2340**. A duplicate of this sheet is attached.

18. CORRESPONDENCE ADDRESS

ARMSTRONG, WESTERMAN, HATTORI
McLELAND & NAUGHTON
1725 K Street, N.W. Suite 1000
Washington, D.C. 20006
Telephone: (202) 659-2930
Facsimile: (202) 887-0357

SUBMITTED BY	
Typed or Printed Name William F. Westerman	Reg. No. 29,988
Signature	Date: May 26, 1999

WFW/yap

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Hidefumi OKADA**

Serial No.: **Not Yet Assigned**

Filed: **May 26, 1999**

For: **DIGITAL CAMERA**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

May 26, 1999

Sir:

Prior to the calculation of the filing fees of the above application, please amend the application as follows:

IN THE CLAIMS:

Please cancel claims 1 through 12 in the application without prejudice or disclaimer and add the following new claims 13 through 36:

--13. A digital camera, comprising:

an image sensor for taking a subject and outputting original image data by a scan scheme;

a main memory;

an original writing circuit for writing said original image data to said main memory;

a processor for creating a thumbnail image data based on said original image data;

a buffer;

a first thumbnail writing circuit for writing to said buffer thumbnail image data outputted from said processor; and

a second thumbnail writing circuit for writing to said main memory thumbnail image data stored in said buffer each time a first predetermined lines of original image data is written to said main memory.--

--14. A digital camera according to claim 13, wherein

a second predetermines lines of thumbnail image data is associated with said first predetermined lines of original image data, and

said buffer including a thumbnail area to store said second predetermined lines of thumbnail image data.--

--15. A digital camera according to claim 13, further comprising a horizontal counter to count a horizontal number of pixels of said original image data and output a horizontal count value, and

a vertical counter to count a vertical number of lines of said original image data and output a vertical count value.--

--16. A digital camera according to claim 15, wherein

said processor includes an extracting circuit to extract predetermined pixel data from said original image data based on said horizontal count value and said vertical count value.--

--17. A digital camera according to claim 16, wherein

said extracting circuit includes a plurality of registers to shift said original image data by a predetermined number of pixels a time and a register controller to intermittently enable said registers based on said horizontal count value and said vertical count value.--

--18. A digital camera according to claim 15, wherein

said first thumbnail writing circuit includes a data writing cricuit to write said thumbnail image data to said buffer based on said horizontal count value and said vertical count value.--

--19. A digital camera according to claim 15, wherein

said first thumbnail writing circuit includes a request output circuit to output a request or read out said thumbnail image data when said vertical counter counts up the number of lines corresponding to said first predetermined lines and said horizontal counter counts up the horizontal number of pixels on said original image data.--

--20. A digital camera according to claim 19, wherein

said second thumbnail writing includes a thumbnail reading circuit to read said thumbnail image data out of said buffer in response to said read request.--

--21. A digital camera according to claim 13, wherein

said original writing circuit includes a first original writing circuit to write said original image data by a predetermined number of pixels a time, and a second original writing circuit to write original image data stored in said buffer to said main memory by said predetermined number of pixels a time.--

--22. A digital camera according to claim 21, wherein

said buffer includes an original area to store at least said predetermined number of pixels of original image data.--

--23. A digital camera according to claim 13, wherein

said main memory is an SDRAM.--

--24. A digital camera according to claim 13, further comprising a recorder to record original image data and thumbnail image data stored in said main memory to a recording medium.--

--25. A digital camera, comprising:

a picture taking means for taking a subject and outputting original image data by a raster scan scheme;

a main memory;

an original writing means for writing said original image data to said main memory;

a creating means for creating a thumbnail image data based on said original image data;

a buffer;

a first thumbnail writing means for writing to said buffer thumbnail image data outputted from said creating means; and

a second thumbnail writing means for writing to said main memory thumbnail image data stored in said buffer each time a first predetermined lines of original image data is written to said main memory.--

--26. A digital camera according to claim 25, wherein

a second predetermines lines of thumbnail image data is associated with said first predetermined lines of original image data, and

said buffer including a thumbnail area to store said second predetermined lines of thumbnail image data.--

--27. A digital camera according to claim 25, further comprising a horizontal counter to count a horizontal number of pixels of said original image data and output a horizontal count value, and

a vertical counter to count a vertical number of lines of said original image data and output a vertical count value.--

--28. A digital camera according to claim 27, wherein

said creating means includes an extracting means to extract predetermined pixel data from said original image data based on said horizontal count value and said vertical count value.--

--29. A digital camera according to claim 28, wherein

said extracting means includes a plurality of registers to shift said original image data by a predetermined number of pixels a time and an enabling means to intermittently enable said registers based on said horizontal count value and said vertical count value.--

--30. A digital camera according to claim 27, wherein

said first thumbnail writing means includes a data writing means to write said thumbnail image data to said buffer based on said horizontal count value and said vertical count value.--

--31. A digital camera according to claim 27, wherein

said first thumbnail writing means includes a request output means to output a request to read out said thumbnail image data when said vertical counter counts up the number of lines corresponding to said first predetermined lines and said horizontal counter counts up the horizontal number of pixels on said original image data.--

--32. A digital camera according to claim 31, wherein

said second thumbnail writing means includes a thumbnail reading means to read said thumbnail image data out of said buffer in response to said read request.--

--33. A digital camera according to claim 25, wherein

said original writing means includes a first original writing means to write said original image data by a predetermined number of pixels a time, and a second original writing means to write original image data stored in said buffer to said main memory by said predetermined number of pixels a time.--

--34. A digital camera according to claim 33, wherein

said buffer includes an original area to store at least said predetermined number of pixels of original image data.--

--35. A digital camera according to claim 25, wherein

said main memory is an SDRAM.--

--36. A digital camera according to claim 25, further comprising a recording means to record original image data and thumbnail image data stored in said main memory to a recording medium.--

REMARKS

The above amendment is believed to place the claims in better condition for examination. Early and favorable action is awaited.

In the event there are any additional fees required, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI, McLELAND & NAUGHTON

Atty. Docket No. 990531
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
Tel: (202) 659-2930
WFW/yap

William F. Westerman
Reg. No. 29,988

TITLE OF THE INVENTION

Digital Camera

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates to digital cameras and, more particularly, to a digital camera adapted to record photographic original image data and thumbnail image data corresponding thereto.

Description of the prior art

Exif is one of recording formats for digital cameras. With this recording format, there is necessity to record not only picture-taking image data (original image data) with desired resolution but also thumbnail image data corresponding to the original image data. Due to this, in the conventional digital camera the CPU has been required to create thumbnail image data from original image data in accordance with a program.

However, where creating such thumbnail image data by using a program, it takes a long time thus increasing the time required to complete one time of picture taking.

SUMMARY OF THE INVENTION

Therefore, it is a primary object of the present invention to provide a digital camera which is capable of reducing a time required for one time of picture taking.

According to the present invention, a digital camera comprises: a picture taking means for taking a subject and outputting original image data by a raster scan scheme; a main memory; an original writing means for writing the original image data to the main memory; a creating means for creating a thumbnail image data based on the original image data; a buffer; a first thumbnail writing means for writing to the buffer thumbnail

image data outputted from the creating means; and a second thumbnail writing means for writing to the main memory thumbnail image data stored in the buffer each time a first predetermined lines of original image data is written to the main memory.

If original image data is outputted through a raster scan scheme from the picture taking means, the original writing means write this original image data to the main memory. On the other hand, the creating means creates thumbnail image data based on the original image data outputted from the picture taking means. The created thumbnail image data is once written to the buffer by the first thumbnail writing means. The second thumbnail writing means writes the thumbnail image data stored in the buffer to the main memory each time a first predetermined lines of original image data is written to the main memory.

According to the present invention, the thumbnail data stored in the buffer is written to an SDRAM each time the first predetermined lines of original image data is written to the SDRAM. The writing operation to the SDRAM 1-sheet of original image data and 1-sheet of thumbnail image data completes within a 1-frame period of time. It is therefore possible to reduce a time required for one time of picture taking.

In a certain aspect of the present invention, a second predetermines lines of thumbnail image data is associated with the first predetermined lines of original image data, and the buffer including a thumbnail area to store the second predetermined lines of thumbnail image data.

In another aspect of the present invention, a horizontal counter counts a horizontal number of pixels of the original image data and outputs a horizontal count value, and a vertical counter counts a vertical number of lines of the original image data and outputs a vertical count value.

In one embodiment of the present invention, the creating means includes an

extracting means to extract predetermined pixel data from the original image data based on the horizontal count value and the vertical count value. The extracting means includes a plurality of registers to shift the original image data by a predetermined number of pixels a time and an enabling means to intermittently enable the registers based on the horizontal count value and the vertical count value.

In another embodiment of the present invention, the first thumbnail writing means includes a data writing means. This data writing means writes the thumbnail image data to the buffer based on the horizontal count value and the vertical count value.

In still another embodiment of the present invention, the first thumbnail writing means includes a request output means. The request output means outputs a request to read out the thumbnail image data when the vertical counter counts up the number of lines corresponding to the first predetermined lines and the horizontal counter counts up the horizontal number of pixels on the original image data. The second thumbnail writing means includes a thumbnail reading means to read the thumbnail image data out of the buffer in response to the read request.

In further aspect of the present invention, the original writing means includes a first original writing means to write the original image data by a predetermined number of pixels a time, and a second original writing means to write original image data stored in the buffer to the main memory by the predetermined number of pixels a time.

The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing one embodiment of the present invention;

Figure 2 is a block diagram showing one part of a timing generator;

Figure 3 is an illustrative view showing a buffer;

Figure 4 is a timing chart showing one part of operation of the Figure 1 embodiment;

Figure 5 is a block diagram showing a memory control circuit;

Figure 6 is a block diagram showing one part of the Figure 5 embodiment;

Figure 7 is a timing chart showing another part of operation of the Figure 1 embodiment; and

Figure 8 is a timing chart showing another part of operation of the Figure 1 embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a digital camera 10 in this embodiment includes a CCD imager 12 which has the effective number of pixels of horizontally 640 pixels by vertically 480 lines. The CCD imager 12 is mounted, at its front, with a primary color filter (not shown) so that a subject optical image is given to the CCD imager 12 through this primary color filter.

If a shutter button 70 is operated, a system controller 68 supplies a control signal to a CPU 56 via an interrupt terminal 56a. The CPU 56, when a 1-frame time period has elapsed from operating the shutter button 70, disables the CCD imager 12. In concrete, a timing generator 13 is suspended from reading charges from the CCD imager 12. As a result, after operating the shutter button 70, 1 frame of camera signal only is outputted from the CCD imager 12.

The outputted camera signal is a progressive scan signal having any one of R, G and B primary color components on each pixel. This camera signal is subjected to well-

known noise removal and level adjustment by a CDS/AGC circuit 14, and then converted into digital-signal camera data by an A/D converter 16 operating at a clock rate of 12 MHz. A signal processing circuit 18 performs YUV conversion with a ratio of 4:2:2 on the camera data outputted from the A/D converter 16, thereby creating YUV data, or original data having 640 pixels × 480 lines.

Incidentally, the timing generator 13 creates a timing signal based on horizontal and vertical synchronizing signals outputted from a signal generator 15, to drive the CCD imager 12 by a progressive scan scheme.

The signal processing circuit 18 also carries out a signal processing as described above at the clock rate 12 MHz, in response to the horizontal and vertical synchronizing signals from the signal generator 15. As a result, Y data as shown in Figure 4(B) and UV data as shown in Figure 4(C) are simultaneously outputted through respective two signal routes. Incidentally, each of the Y data, U data and V data has 8 bits per pixel.

The Y data is inputted, on a pixel-by-pixel basis, to four D-FF circuits 20a – d20d that are in serial connection. The D-FF circuits 20a – 20d has their outputs to be simultaneously inputted to a D-FF circuit 28. That is, 4 pixels in a horizontal direction, or 32 bits, of Y data are simultaneously inputted to the D-FF circuit 28. On the other hand, U data and V data are outputted alternately from the signal processing circuit 18, every 8 bits. Due to the conversion of 4:2:2, the Y data and the V data each have a data amount of a half of that 1/2 of the Y data. Accordingly, in a duration that 4 pixels of Y data are outputted through one signal route, 2 pixels of Y data and 2 pixels of V data are outputted through the other signal route. The 2 pixels of UV data are also simultaneously inputted to a D-FF circuit 30 via D-FF circuits 22a – 22d. The D-FF circuits 28 and 30 operate at a clock rate of 3 MHz so that Y data and UV data are respectively outputted from the D-FF circuits 28 and 30 in timing as shown in Figure 4(D) and (E) and every 32 bits.

The Y data outputted from the signal processing circuit 18 is also inputted with a 1-pixel delay to a D-FF circuit 24b by way of a D-FF circuit 24a which is enabled at all times and operates at the clock rate 12 MHz. The D-FF circuit 24b as well as D-FF circuits 24c – 24e connected serial in the rear stage are to be enabled by an enable signal RegEN outputted from the timing generator 13. That is, these circuits latch input data responsive to a 12-MHz clock only while the enable signal RegEN shown in Figure 4(F) is high in level. The respective ones of Y data latched by these D-FF circuits 24b – 24e are simultaneously inputted to a D-FF circuit 32 where they are latched responsive to the same enable signal RegEN.

As can be understood from Figure 4(F), the enable signal RegEN rises every 8 pixels with a result that Y data is inputted once per 8 pixels to the D-FF circuit 32. That is, 1 pixel of Y data is extracted from among consecutive 8-pixels Y data. The D-FF circuit 32 also responds to the enable signal RegEN and latches input data corresponding to predetermined 4 pixels. As a result, Y data each having 8 pixels is outputted in timing as shown in Figure 4(H) from the D-FF circuit 32. Incidentally, with respect to a vertical direction, operation is once per 8 lines or more.

The UV data outputted from the signal processing circuit 18 is inputted to a selector 27 directly or via a D-FF circuit 26a. The D-FF circuit 26a is enabled at all times to operate at the 12-MHz clock rat whereby the Y data and V data of same pixels are simultaneously inputted to the selector 27. The selector 27 selects any of input data depending on a select signal UVSEL to be outputted from the timing generator 13. The selector 27 is serially connected with D-FF circuits 26b – 26e each of which latches input data responsive to the 12-MHz clock only when the enable signal RegEN is at a high level. A D-FF circuit 34 also latches input data in response to the enable signal RegEN. As a result, the D-FF circuits 26b – 26e have respective outputs to be simultaneously

outputted through the D-FF circuit 34.

The select signal UVSEL varies in level every 8 pixels, as shown in Figure 4(G). If the select signal UVSEL is at a low level, the selector 27 selects an output of the D-FF circuit 26a. When the select signal UVSEL is at a high level, the selector 27 selects an output of the signal processing circuit 18. The enable signal RegEN rises only once per 8 pixels as stated before. As a result, the U data and the V data are alternatively latched by each of the D-FF circuits 26b – 26e. That is, the U data and the V data are alternately extracted every 8 pixels. The extracted UV data corresponding to predetermined 4 pixels is outputted in timing as shown in Figure 4(I) from the D-FF circuit 34. Incidentally, with respect to the vertical direction, the above operation is carried out every 8 lines also on the UV data.

In this manner, pixel data is extracted every 8 pixels and lines respectively in the horizontal and vertical directions. As a result, thumbnail image data formed by 80 pixels × 60 lines is created from 640 pixels × 480 lines of original image data.

A switch SW1 is switched in accordance with a select signal SDSEL outputted from the timing generator 13. That is, if the select signal SDSEL is at "0", the switch SW1 is connected to the D-FF circuit 28. If the select switch SDSEL is at "1", the switch SW1 is connected to the D-FF circuit 30. Also, when the select signal SDSEL assumes "2" and "3", the switch SW1 is connected respectively to the D-FF circuits 32 and 34. The select signal SDSEL responds to the 12-MHz clock and varies in the order of "0", "2", "1" and "3", as shown in Figure 4(J). As a result, outputs are selected in the order of the D-FF circuit 28, D-FF circuit 32, D-FF circuit 30 and D-FF circuit 34. Thus, original image data and thumbnail image data are outputted in timing shown in Figure 4(K) through the switch SW1.

The connections of the switch SW1 to the D-FF circuits 32 and 34 are respectively

effective only during a time period that the Y data and UV data corresponding to the predetermined 4 pixels are respectively outputted from the D-FF circuits 32 and 34. For this reason, in Figure 4(K) the outputs of the switch SW1 during ineffective connection are shown by hatching. As can be understood from Figure 4(K), in a duration that 32-pixels original image data is outputted through the switch SW1, 4 pixels of thumbnail image data associated with that 32 pixels are outputted through the switch SW1.

A buffer 36 is configured by an SRAM with dual ports, as shown in Figure 3. The SRAM has a total word number of "128". A former half of 64 words constitutes an original area to store original image data, while a latter half of 64 words includes predetermined 40 words constituting a thumbnail area to store thumbnail image data.

Explaining in greater detail, each word has a 32-bit width of 32 bits. The original area assigned with addresses "0" – "63" is divided into two banks. That is, each bank can store 64 pixels of YUV data. Accordingly, the original image data outputted through the switch SW1 is alternately written by 64 pixels a time onto the banks 1 or 2. Read out is carried out from a bank not being written thereon.

On the other hand, thumbnail image data is stored to an address "64" – "83" and address "96" – "115". This area with capacity of totally 40 words is given as a thumbnail area. In also the thumbnail area each word has a width of 32 bits and the Y data or UV data corresponding to predetermined 4 pixels is written onto 1 word. Specifically, Y data is written onto 20 words of the addresses "64" – "83", while UV data is onto 20 words of the addresses "96" – "115". In this manner 80-pixels, or 1-line, thumbnail image data is written to the thumbnail area.

The timing generator 13 also provides a write address signal shown in Figure 4(L) and a write enable signal shown in Figure 4(M) to the buffer 36. By varying the select signal SDSEL as shown in Figure 4(J), the original image data and the thumbnail image

data are outputted in the timing shown in Figure 4(K) from the switch SW1. Due to this, the output timing of the write enable signal varies from 12 MHz to 24 MHz only when effective thumbnail image data is being outputted. As a result, the original image data and the thumbnail image data are written to write addresses shown in Figure 4(L). In this manner, in a duration that the 32-pixels original image data is written to the original area, the associated 4-pixels thumbnail image data is written to the thumbnail area.

The 64-pixels original image data written in one bank of the original area is read out in concurrent with the writing of the succeeding 64-pixels original image data onto the other bank. Specifically, the timing generator 13 provides an original read request shown in Figure 7(B) to the memory control circuit 40. The memory control circuit 40, in turn, reads original image data out of a predetermined bank in response to this original read request. The memory control circuit 40, as shown in Figure 7(E), outputs an address signal at a rate of 24 MHz and reads original data from the original area as shown in Figure 7(D).

Referring to Figure 5, the original read request is inputted to a mediation circuit 40a through the RS-FF circuit 40b. The mediation circuit 40a also receives other requests from the RS-FF circuits 40c – 40e and mediates between the requests. In order to respond to any of the requests, the mediation circuit 40a outputs a predetermined start signal to a processing circuit 40f.

The processing circuit 40f is configured as shown in Figure 6. A bus 38 includes data buses 38a – 38c, an address bus 38d and a control bus 38e. The data buses 38a and 38b are respectively connected to input terminals of 3-state buffers 40i and 40j. The data bus 38c is commonly connected to the output terminals of the 3-state buffers 40i, 40j and the input terminal of the D-FF circuit 40k. The address bus 38d and the control bus 38e are connected to the buffer control circuit 40g.

D-FF circuits 40k and 40p are in serial connection. The D-FF circuit 40p has an output terminal connected to an input terminal of a 3-state buffer 49. The 3-state buffer 49 has an output terminal connected to an SDRAM (synchronous DRAM) 44 through a data bus 42a included in a bus 42. D-FF circuits 40r – 40u serially connected one another are inserted between the output terminal of the 3-state buffer 49 and an input terminal of a 3-state buffer 40v. The 3-state buffers 40i, 40j and 40v are turned on/off by a buffer control circuit 40g, while the 3-state buffer 49 is turned on/off by an SDRAM control circuit 40h.

When processing an original read request from the timing generator 13, the processing circuit 40f outputs an address signal shown in Figure 8(B) to the buffer 36 in response to a start signal shown in Figure 8(A), and reads original image data (YUV data) shown in Figure 8(C) from the original area of the buffer 36. The read YUV data is written by DMA (Direct Memory Access) to the SDRAM 44. At this time, the processing circuit 40f carries out the processing at the 24-MHz clock rate.

Explaining in detail, the buffer control circuit 40g outputs the above address signal via an address bus 38d, and making a chip select signal CS1 low in level and turn on the 3-state buffer 40j. Furthermore, the SDRAM control circuit 40h causes the 3-state buffer 49 to turn on. Due to this, the original image data read from the buffer 36 is outputted in timing shown in Figure 8(H) to the SDRAM 44 via the D-FF circuits 40k – 40p. That is, because four D-FF circuits 40k – 40p are interposed between the 3-state buffers 40i and 40q, the fetched YUV data is outputted with a 4-clock delay to the SDRAM 44.

The SDRAM control circuit 40h also outputs an address signal, RAS signal and CAS signal shown in Figure 8(D) – (F) to the SDRAM 44. The address signal is outputted to the SDRAM 44 through an address bus 42b, while the RAS signal and the CAS signal are outputted through control busses 42c and 42d. The address signal first

designates a row address and then designates, during a succeeding 4-clock time period, a column address. The RAS signal falls simultaneously with the designation of a row address, whereas the CAS signal falls at a time point that a column address is designated. This causes the SDRAM 44 to acknowledge 4 addresses and writes 32 bits per address the YUV data shown in Figure 6(H) to desired 4 addresses. This operation is carries out for 64 pixels.

The processing circuit 40f supplies an end signal to the mediation circuit 32a each time 64-pixels original image data writing has been completed. The mediation circuit 32a enters to a process for a next request. By processing 10 times an original read request from the timing generator 13 in this manner, 640 pixels or 1 line of original image data are written to the SDRAM 44. If the original read request is repeated 480 times, 1 screen of original image data is obtained within the SDRAM 44.

The timing generator 13 outputs a thumbnail read request each time 80 pixels of thumbnail image data are obtained within the buffer 36 or at an interval of 8 lines. The thumbnail read request is outputted simultaneous with a 10-th original read request for a predetermined line as shown in Figure 7(C), which is supplied to an RS-FF circuit 40c shown in Figure 5. The mediation circuit 40a processes the thumbnail read request following the 10-th original read request. In processing the thumbnail read request, a predetermined start signal is also supplied from the mediation circuit 40a to the processing circuit 40f. The buffer control circuit 40g supplies an address signal shown in Figure 7(E) to the buffer 36. Due to this, thumbnail image data shown in Figure 7(D) is read out of the thumbnail image area, and this thumbnail image data is written to the SDRAM 44 in a manner similar to the above.

Because the thumbnail area stores 1 line of thumbnail image data, the processing the thumbnail read request by once results in writing of 1-line thumbnail image data onto

the SDRAM 44. Such writing of thumbnail image data is carried out at an interval of 8 lines. In other words, each time 640 pixels × 8 lines of original image data are written to the SDRAM 44, 80 pixels × 1 line of thumbnail image data are written to the SDRAM 44. Accordingly, writing is completes on 64 pixels × 480 lines of original image data as well as 80 pixels × 60 lines of thumbnail image data, before elapsing a 1-frame time period from depressing the shutter button 70.

Incidentally, the thumbnail image data is written to the SDRAM 44 during a horizontal blanking period shown in Figure 7(A). Consequently, the writing of thumbnail image data has no adverse effect upon the writing of original image data.

The timing generator 13 is configured as shown in Figure 2. An H counter 13a is incremented responsive to the 12-MHz clock and reset by the horizontal synchronizing signal. That is, the H counter 13a counts the horizontal number of pixels of the original image data. The H counter 13a has a count value represented by 10 bits. The lower 3 bits [2:0] of such a count value is inputted to a decoder 13b, and a lower third bit [2] is inputted to D-FF circuit 13c. Also, lower 2 bits [1:0] are inputted to a decoder 13e and inverter 13f, and lower 5 bits [4:0] are inputted to a decoder 13g.

The decoder 13b, when the 3-bits input data represents "1", has a high output level. Such an output of the decoder 13b is used as an enable signal RegEN. Also, the lower third bit data inputted to the D-FF circuit 13c is outputted as a select signal UVSEL through a next-stage D-FF circuit 13d. The decoder 13e, when its 2-bits input data represents "0", "1", "2", and "3", creates select signals SDSEL respectively representing "0", "2", "1" and "3". As a result, the enable signal RegEN varies as shown in Figure 4(F), the select signal UVSEL as shown in Figure 4(G), and the select signal SDSEL as shown in Figure 4(J).

The inverter 13f inverts its input data, and the decoder 13g outputs a high level

signal when its 5-bit data represents "25" – "28". Also, the inverter 13i inverts the 24-MHz clock. A V counter 13n is incremented responsive to the horizontal synchronizing signal and reset by the vertical synchronizing signal. That is, the V counter 13n counts the vertical number of lines of the original image data. The V counter 13n has a count value represented by 9 bits. Among these, the lower 3 bits [2:0] are inputted to a decoder 13m. The decoder 13m outputs a high level signal only when this input represents "1". That is, the output of the decoder 13m becomes high in level every 8 lines.

The outputs of the decoders 13g and 13m are ANDed by an AND circuit 13k. The AND circuit 13k has an output which is ORed with an output of the inverter 13f by an OR circuit 13h. Further, the OR circuit 13h has an output which is ANDed with an output of the inverter 13i by an AND circuit 13j. As a result, a write enable signal shown in Figure 4(M) is obtained from the AND circuit 13j, being outputted to the buffer 36.

Address generating circuits 13p – 13s determine respective write addresses of the original Y data, the original UV data, the thumbnail Y data and the thumbnail UV data based on count values of the H counter 13a, and input the address signals to a selector 13t. The selector 13t also receives the lower 2bits of the H counter 13a count value as a control signal, and selects any of the address signals. That is, when the control signal shows "0", it selects an output of the address generating circuit 13p. When the control signal shows "2", an output of the address generating circuit 13q is selected. Also, when the control signal represents "1", an output of the address generating circuit 13r is selected. When the control signal represents "3", an output of the address generating circuit 13s is selected. As a result, the address signal varies as shown in Figure 4(L).

In this manner the original image data and thumbnail image data are written to a predetermined address in accordance with the write enable signal and address signal given from the timing generator 13 to the buffer 36.

Read request generating circuits 13u and 13v receive both count values of the H counter 13a and the V counter 13m, and output respective original read request and thumbnail read request in predetermined timing. Explaining in more detail, the read request generating circuit 13u outputs an original read request whenever the H counter 13a counts 64 pixels on each line. On the other hand, the read request generating circuit 13v outputs a thumbnail read request each time the V counter 13m counts 7 lines and the H counter 13a counts 640 pixels. As a result original read requests are outputted at an interval of 64 pixels as shown in Figure 7(B). Also, a thumbnail read request is outputted simultaneous with a 10-th original read request on a predetermined line.

If 1 screen of original image data and thumbnail image data is obtained within the SDRAM 44, a JPEG compression/decompression circuit 48 shown in Fig. 1 sends write and read requests to the memory control circuit 40. The write request is to demand writing of original image data and thumbnail image data onto the buffer 46, while the read request is to demand reading of compressed data written on the buffer 50. Accordingly, requests are given in the order of a write request and a read request.

The mediation circuit 40a receives a write request via the RS-FF circuit 40d and supplies a corresponding start signal to the processing circuit 40f. A buffer control circuit 40g shown in Figure 6 makes the chip select signal CS2 low in level and reads original image data from the SDRAM 44 in a procedure similar to the above. The read original image data is outputted to the buffer 46 via the D-FF circuits 40r – 40v and 3-state buffer 40p. The buffer control circuit 40g also outputs the address signal and write enable signal to the buffer 46. Due to this, the original image data is written to a predetermined address of the buffer 46.

The JPEG compression/decompression circuit 48 performs JPEG compression on the original image data written on the buffer 46 and writes the compressed data to a buffer

50. In this manner, the compressed data stored in the buffer 50 is read out by the memory control circuit 40 in response to a read request from the JPEG compression/decompression circuit 48, being again written to the SDRAM 44.

That is the mediation circuit 40a inputs a predetermined start signal to the processing circuit 40f in response to a read request outputted through the RS-FF circuit 40e. Receiving this, the buffer control circuit 40g of Figure 6 makes a chip select signal CS3 low in level and outputs an address signal to the buffer 50. Also, the SDRAM control circuit 40h brings the 3-state buffer 49 to an on state and inputs the address signal, the RAS signal and the CAS signal in predetermined timing to the SDRAM 44. Due to this, the compressed data stored in the buffer 50 is stored to predetermined address of the SDRAM 44.

Such a process is made also on the thumbnail image data. As a result, 1 screen of compressed data of both the original image and thumbnail image is obtained in the SDRAM 44.

The CPU 56 fetches this compressed data via a bus bridge 52 and bus 54 and writes it to a DRAM 58. The CPU 56 thereafter records this compressed data onto a memory card 66 through an I/F circuit 60.

According to this embodiment, each time 8-lines original image data bas been written to the SDRAM 44, 1 line of associated thumbnail image data is written to the SDRAM 44. Accordingly, it is possible to complete the writing of 1-screen original image data and 1-screen thumbnail image data within a 1-frame period. Furthermore, the memory control circuit 40 has a processing speed of 24 MHz which is 4 times the processing speed of the signal processing circuit 18. Consequently, the original image data and thumbnail image data can be compressed and recorded to the memory card 66 in concurrent with their writing to the SDRAM. As a result, in concurrent with continuous

writing the original image data and thumbnail image data of each frame to the SDRAM 44, the compressed data of each frame can be recorded in a continuous fashion to the memory card 66. In other words, it is possible to record to the memory card 66 an original motion image comprising a plurality of frames of original still pictures and a thumbnail motion image comprising a plurality of frames of thumbnail still pictures.

In this embodiment the thumbnail image data was written line by line to the SDRAM 44 by utilizing a horizontal blanking period. Alternatively, the writing of the thumbnail image data to the SDRAM 44 may be performed every a plurality of lines. In such a case, it is required to increase the capacity of the thumbnail area in order to store a plurality of lines of thumbnail image data. Also, the capacity of the thumbnail area can be increased to 80 pixels $\times$ 60 lines so that 1 screen of thumbnail image data is collectively written to the SDRAM 44 within a vertical blanking period.

Meanwhile, in this embodiment explanation was based on the CCD imager of a progressive scan scheme. This invention, however, is applicable to a digital camera using any of an image sensor of a raster scan scheme. Due to this, an interlace scan method may be adopted in place of the progressive scan method. Also, a CMOS image sensor may be adopted instead of a CCD imager.

Furthermore, the memory card may use a various type of a card including SSFDC (Solid State Floppy Disc Card). Also, in this embodiment explanation was made using a primary color filter arranged in mosaic form with R, G and B. Alternatively, a complementary color filter may be used which is formed by Ye, Cy, Mg and G arranged in a mosaic form. Furthermore, the main memory can use something other than SDRAM provided that burst transfer is possible.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to

be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A digital camera, comprising:

a picture taking means for taking a subject and outputting original image data by a raster scan scheme;

a main memory;

an original writing means for writing said original image data to said main memory;

a creating means for creating a thumbnail image data based on said original image data;

a buffer;

a first thumbnail writing means for writing to said buffer thumbnail image data outputted from said creating means; and

a second thumbnail writing means for writing to said main memory thumbnail image data stored in said buffer each time a first predetermined lines of original image data is written to said main memory.

2. A digital camera according to claim 1, wherein

a second predetermines lines of thumbnail image data is associated with said first predetermined lines of original image data, and

said buffer including a thumbnail area to store said second predetermined lines of thumbnail image data.

3. A digital camera according to claim 1, further comprising a horizontal counter to count a horizontal number of pixels of said original image data and output a horizontal count value, and

a vertical counter to count a vertical number of lines of said original image data and output a vertical count value.

4. A digital camera according to claim 3, wherein

said creating means includes an extracting means to extract predetermined pixel data from said original image data based on said horizontal count value and said vertical count value.

5. A digital camera according to claim 4, wherein

said extracting means includes a plurality of registers to shift said original image data by a predetermined number of pixels a time and an enabling means to intermittently enable said registers based on said horizontal count value and said vertical count value.

6. A digital camera according to claim 3, wherein

said first thumbnail writing means includes a data writing means to write said thumbnail image data to said buffer based on said horizontal count value and said vertical count value.

7. A digital camera according to claim 3, wherein

said first thumbnail writing means includes a request output means to output a request to read out said thumbnail image data when said vertical counter counts up the number of lines corresponding to said first predetermined lines and said horizontal counter counts up the horizontal number of pixels on said original image data.

8. A digital camera according to claim 7, wherein

said second thumbnail writing means includes a thumbnail reading means to read said thumbnail image data out of said buffer in response to said read request.

9. A digital camera according to claim 1, wherein

said original writing means includes a first original writing means to write said original image data by a predetermined number of pixels a time, and a second original writing means to write original image data stored in said buffer to said main memory by said predetermined number of pixels a time.

10. A digital camera according to claim 9, wherein

said buffer includes an original area to store at least said predetermined number of pixels of original image data.

11. A digital camera according to claim 1, wherein

said main memory is an SDRAM.

12. A digital camera according to claim 1, further comprising a recording means to record original image data and thumbnail image data stored in said main memory to a recording medium.

ABSTRACT OF THE DISCLOSURE

A digital camera includes a CCD imager which outputs 640 pixels × 480 lines of camera signal in a raster scan scheme. The camera signal outputted from the CCD imager is subjected to a predetermined signal processing whereby created are 640 pixels × 480 lines of original image data and 80 pixels × 60 lines of thumbnail image data. Both the created original image data and thumbnail image data are written to a SDRAM. The writing of the thumbnail image data is performed during a horizontal blanking period of the original image data. As a result, image data writing operation completes within a 1-frame period of time.

FIG. 1

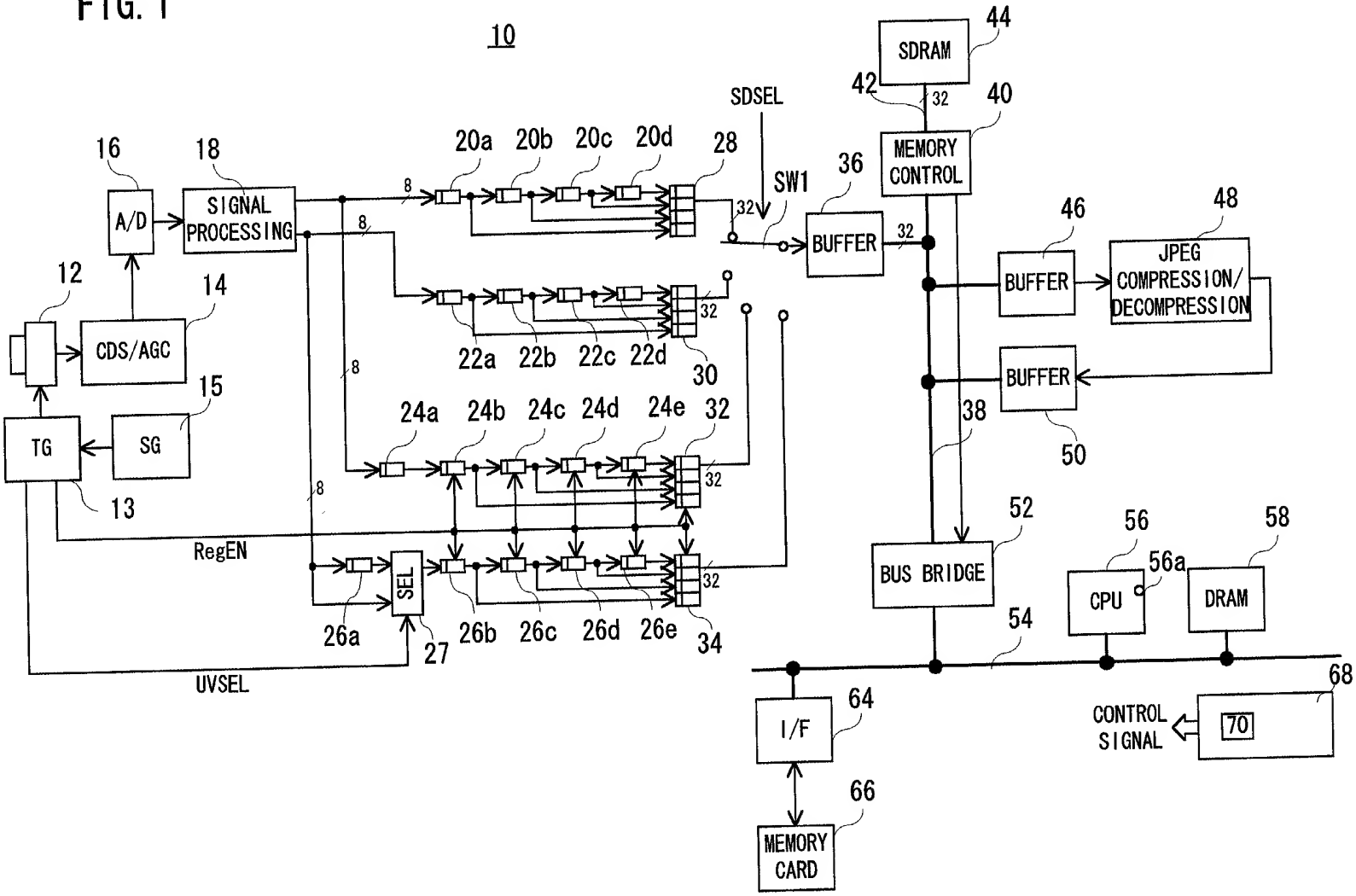

10
SDRAM
44
42
32
40
MEMORY CONTROL
SDSEL
SW1
36
16
18
20a
20b
20c
20d
28
A/D
SIGNAL PROCESSING
8
32
BUFFER
32
46
48
BUFFER
JPEG COMPRESSION/ DECOMPRESSION
12
14
CDS/AGC
22a
22b
22c
22d
30
32
15
24a
24b
24c
24d
24e
32
TG
SG
38
BUFFER
50
13
RegEN
52
56
58
BUS BRIDGE
CPU
56a
DRAM
SEL
26a
26b
26c
26d
26e
34
27
54
UVSEL
64
68
I/F
CONTROL SIGNAL
70
66
MEMORY CARD

FIG. 2

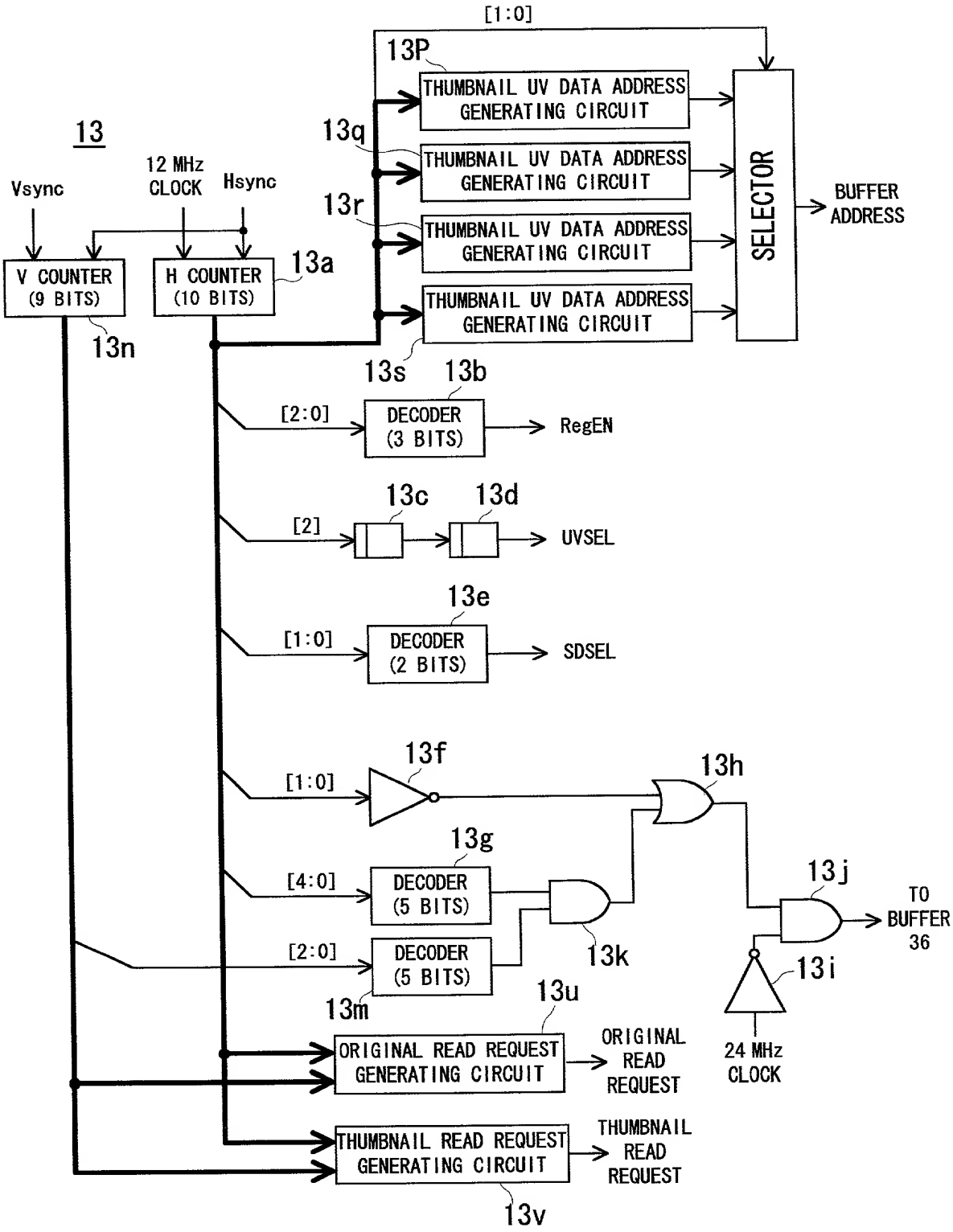

[1:0]
13P
THUMBNAIL UV DATA ADDRESS GENERATING CIRCUIT
13q
THUMBNAIL UV DATA ADDRESS GENERATING CIRCUIT
13r
THUMBNAIL UV DATA ADDRESS GENERATING CIRCUIT
THUMBNAIL UV DATA ADDRESS GENERATING CIRCUIT
SELECTOR
BUFFER ADDRESS
13
Vsync
12 MHz CLOCK
Hsync
V COUNTER (9 BITS)
H COUNTER (10 BITS)
13a
13n
13s
13b
[2:0]
DECODER (3 BITS)
RegEN
13c
13d
[2]
UVSEL
13e
[1:0]
DECODER (2 BITS)
SDSEL
13f
[1:0]
13h
13g
[4:0]
DECODER (5 BITS)
13j
TO BUFFER 36
[2:0]
DECODER (5 BITS)
13k
13i
13m
13u
ORIGINAL READ REQUEST GENERATING CIRCUIT
ORIGINAL READ REQUEST
24 MHz CLOCK
THUMBNAIL READ REQUEST GENERATING CIRCUIT
THUMBNAIL READ REQUEST
13v

FIG. 3

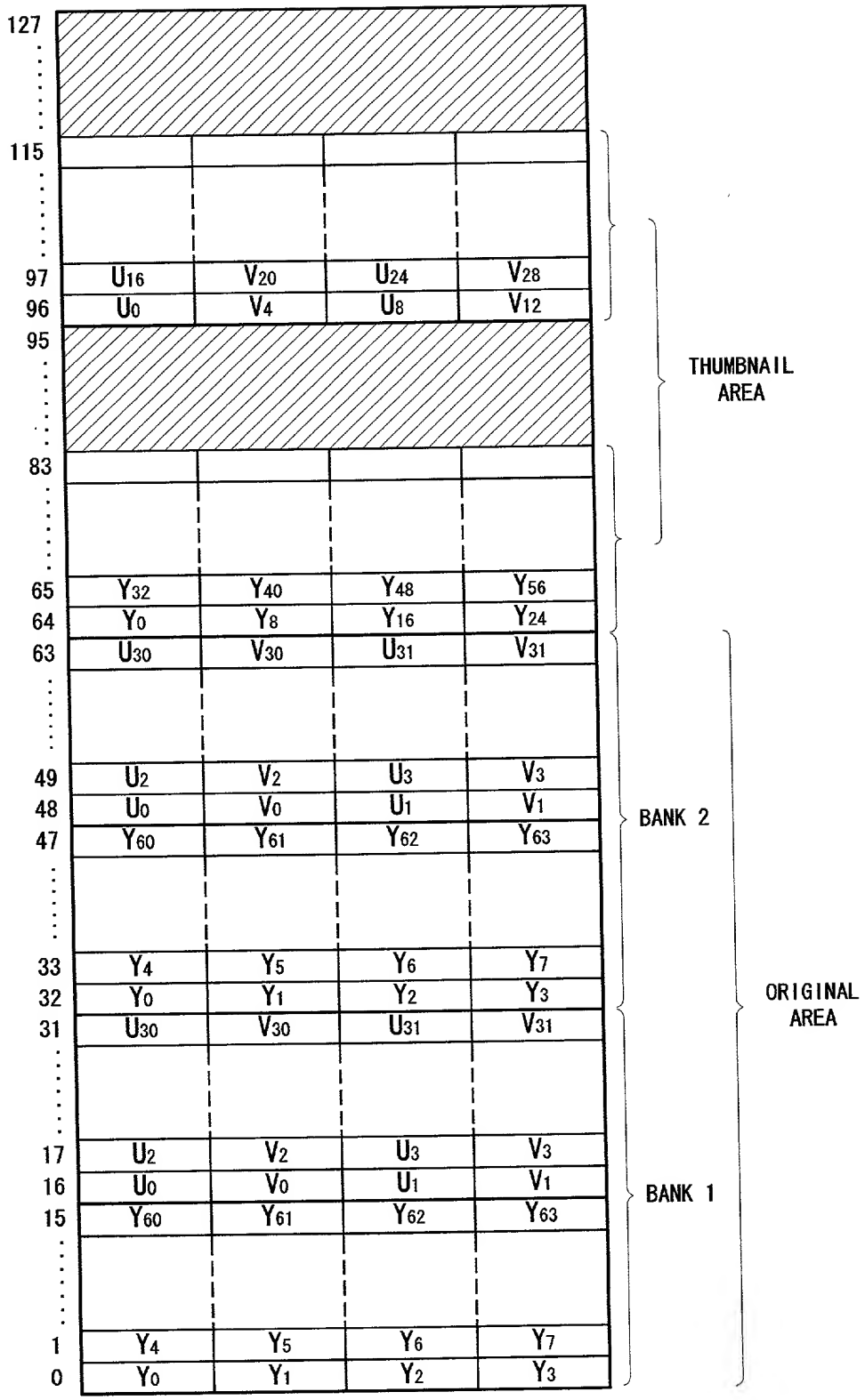

127
115
97
96
95
83
65
64
63
49
48
47
33
32
31
17
16
15
1
0
U16 V20 U24 V28
U0 V4 U8 V12
Y32 Y40 Y48 Y56
Y0 Y8 Y16 Y24
U30 V30 U31 V31
U2 V2 U3 V3
U0 V0 U1 V1
Y60 Y61 Y62 Y63
Y4 Y5 Y6 Y7
Y0 Y1 Y2 Y3
U30 V30 U31 V31
U2 V2 U3 V3
U0 V0 U1 V1
Y60 Y61 Y62 Y63
Y4 Y5 Y6 Y7
Y0 Y1 Y2 Y3
THUMBNAIL AREA
BANK 2
BANK 1
ORIGINAL AREA

FIG. 4

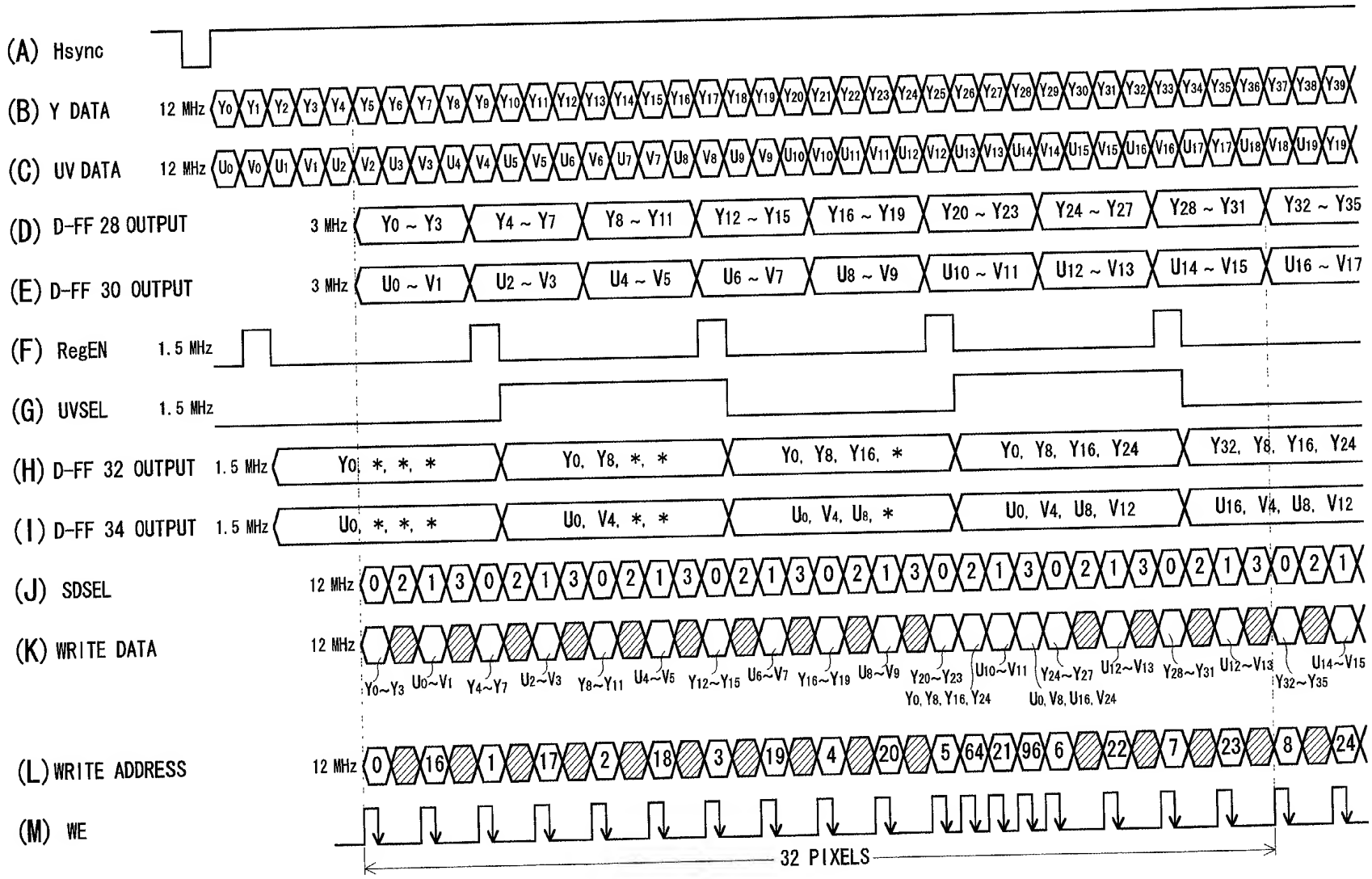

(A) Hsync
(B) Y DATA
12 MHz
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 Y10 Y11 Y12 Y13 Y14 Y15 Y16 Y17 Y18 Y19 Y20 Y21 Y22 Y23 Y24 Y25 Y26 Y27 Y28 Y29 Y30 Y31 Y32 Y33 Y34 Y35 Y36 Y37 Y38 Y39
(C) UV DATA
12 MHz
U0 V0 U1 V1 U2 V2 U3 V3 U4 V4 U5 V5 U6 V6 U7 V7 U8 V8 U9 V9 U10 V10 U11 V11 U12 V12 U13 V13 U14 V14 U15 V15 U16 V16 U17 V17 U18 V18 U19 V19
(D) D-FF 28 OUTPUT
3 MHz
Y0 ~ Y3
Y4 ~ Y7
Y8 ~ Y11
Y12 ~ Y15
Y16 ~ Y19
Y20 ~ Y23
Y24 ~ Y27
Y28 ~ Y31
Y32 ~ Y35
(E) D-FF 30 OUTPUT
3 MHz
U0 ~ V1
U2 ~ V3
U4 ~ V5
U6 ~ V7
U8 ~ V9
U10 ~ V11
U12 ~ V13
U14 ~ V15
U16 ~ V17
(F) RegEN
1.5 MHz
(G) UVSEL
1.5 MHz
(H) D-FF 32 OUTPUT
1.5 MHz
Y0, *, *, *
Y0, Y8, *, *
Y0, Y8, Y16, *
Y0, Y8, Y16, Y24
Y32, Y8, Y16, Y24
(I) D-FF 34 OUTPUT
1.5 MHz
U0, *, *, *
U0, V4, *, *
U0, V4, U8, *
U0, V4, U8, V12
U16, V4, U8, V12
(J) SDSEL
12 MHz
0 2 1 3 0 2 1 3 0 2 1 3 0 2 1 3 0 2 1 3 0 2 1 3 0 2 1 3 0 2 1
(K) WRITE DATA
12 MHz
Y0~Y3
U0~V1
Y4~Y7
U2~V3
Y8~Y11
U4~V5
Y12~Y15
U6~V7
Y16~Y19
U8~V9
Y20~Y23
Y0, Y8, Y16, Y24
U10~V11
Y24~Y27
U0, V8, U16, V24
U12~V13
Y28~Y31
U12~V13
Y32~Y35
U14~V15
(L) WRITE ADDRESS
12 MHz
0 16 1 17 2 18 3 19 4 20 5 64 21 96 6 22 7 23 8 24
(M) WE
32 PIXELS

FIG. 5

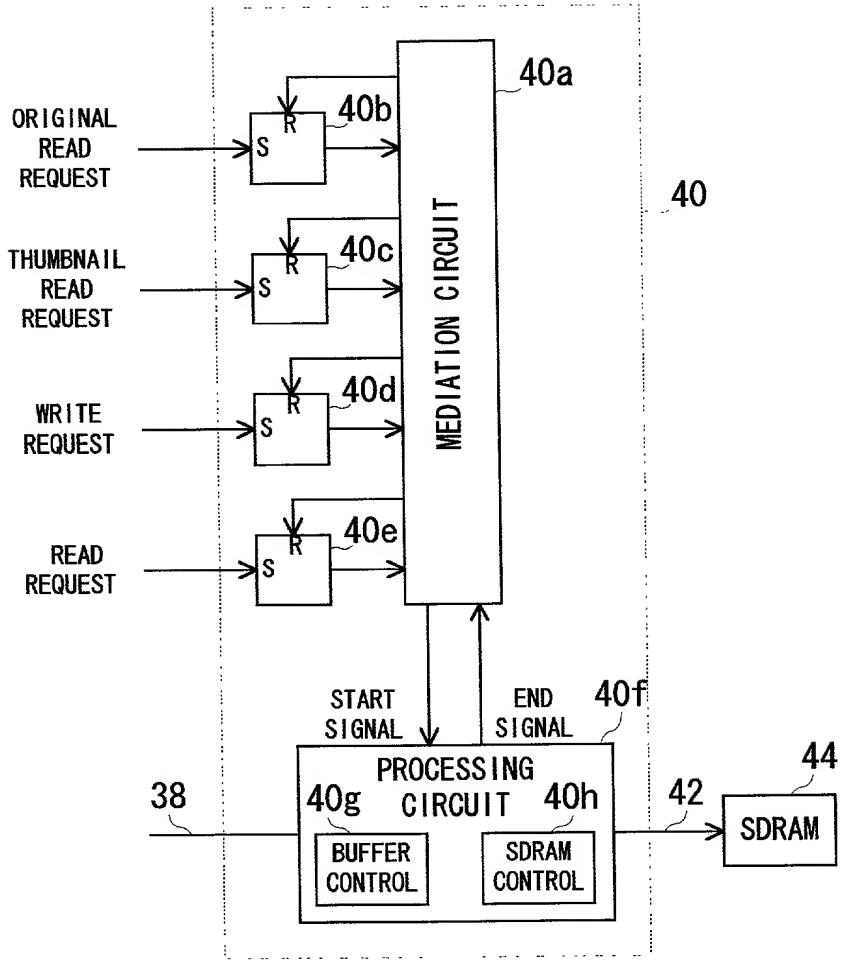

ORIGINAL READ REQUEST
THUMBNAIL READ REQUEST
WRITE REQUEST
READ REQUEST
S
R
40b
40c
40d
40e
40a
MEDIATION CIRCUIT
40
START SIGNAL
END SIGNAL
40f
PROCESSING CIRCUIT
40g
40h
BUFFER CONTROL
SDRAM CONTROL
38
42
44
SDRAM

FIG. 6

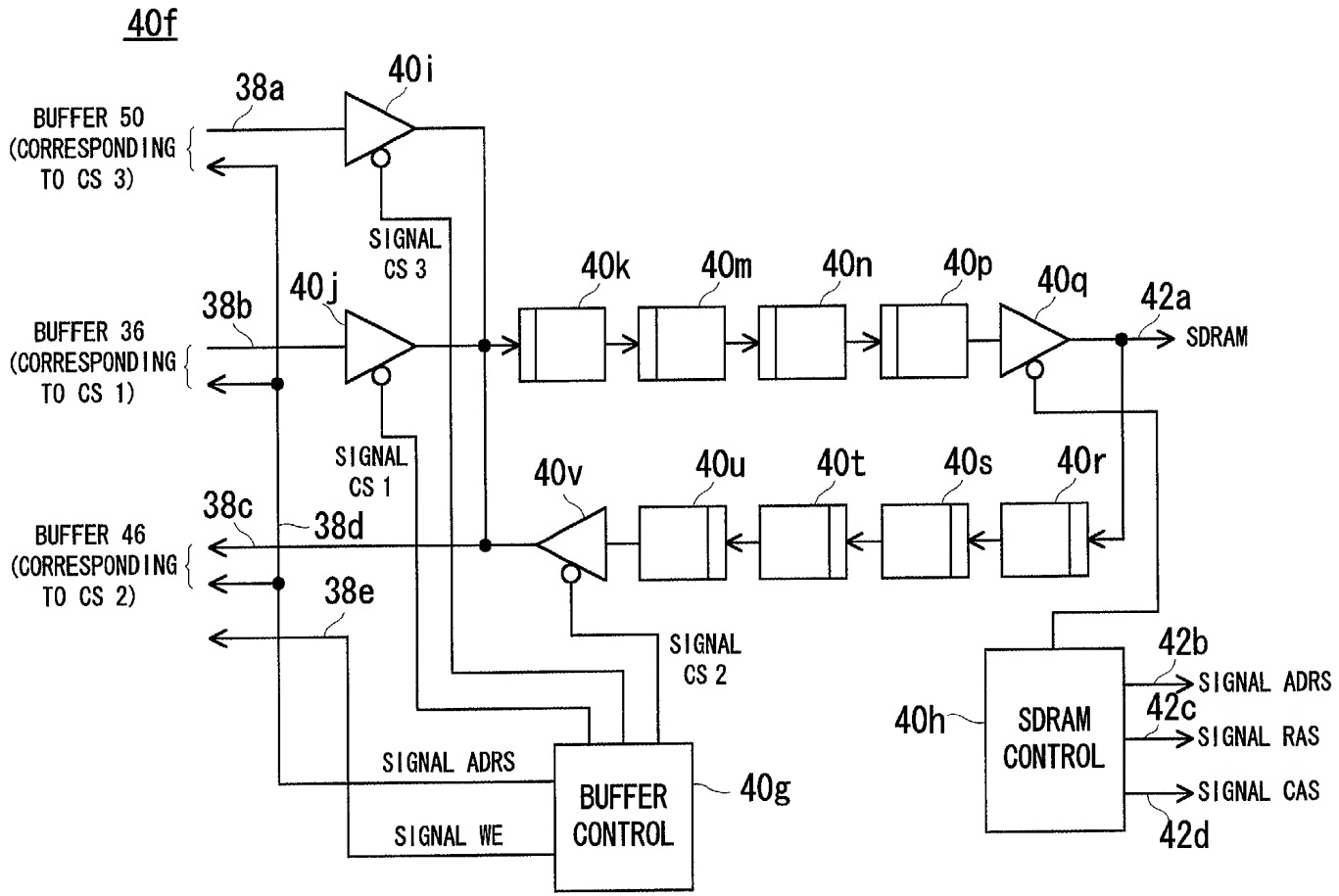

40f
38a
40i
BUFFER 50
(CORRESPONDING
TO CS 3)
SIGNAL
CS 3
40k
40m
40n
40p
40q
42a
SDRAM
38b
40j
BUFFER 36
(CORRESPONDING
TO CS 1)
SIGNAL
CS 1
40v
40u
40t
40s
40r
38c
38d
BUFFER 46
(CORRESPONDING
TO CS 2)
38e
SIGNAL
CS 2
42b
SIGNAL ADRS
40h
SDRAM
CONTROL
42c
SIGNAL RAS
SIGNAL CAS
42d
SIGNAL ADRS
BUFFER
CONTROL
40g
SIGNAL WE

FIG. 7

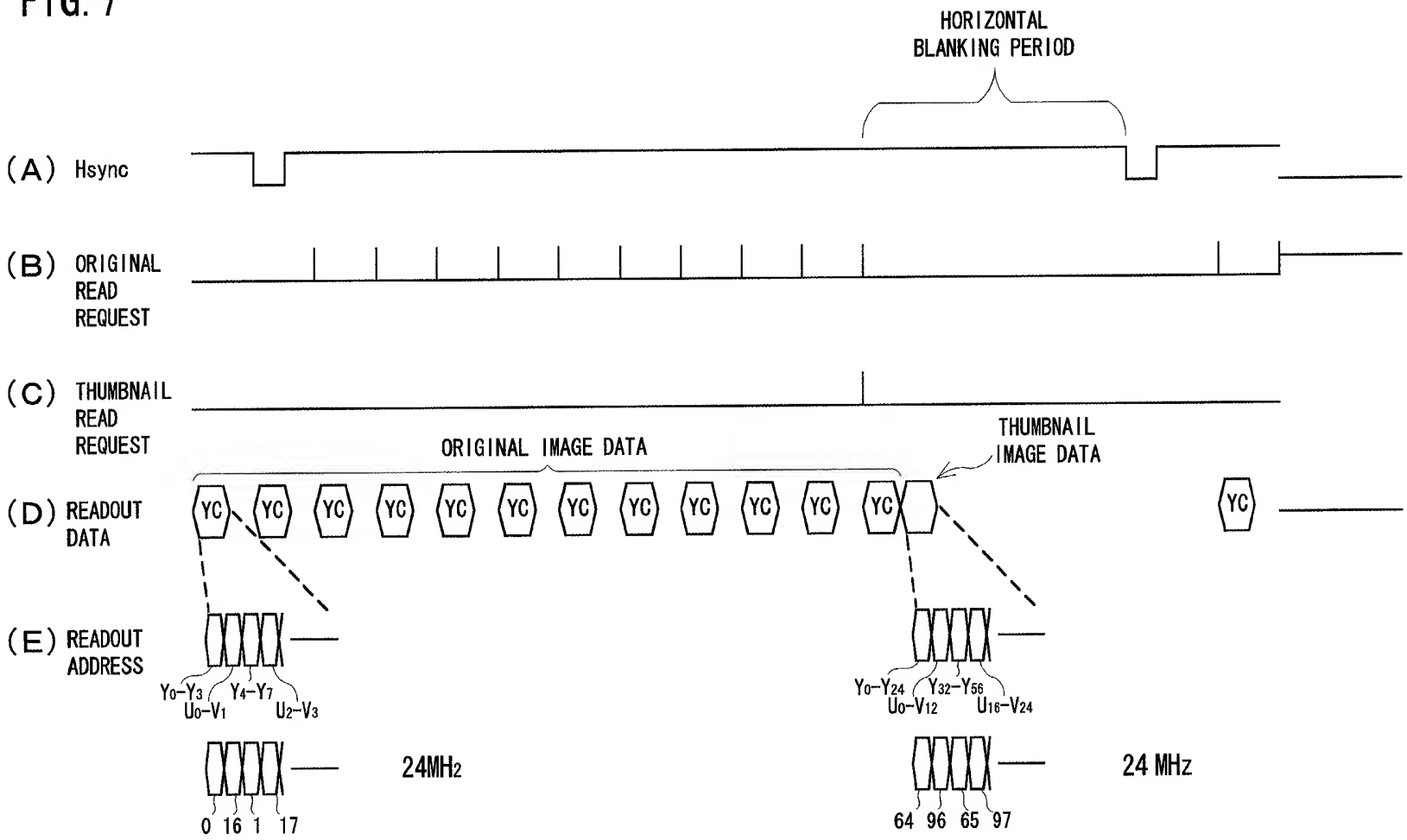
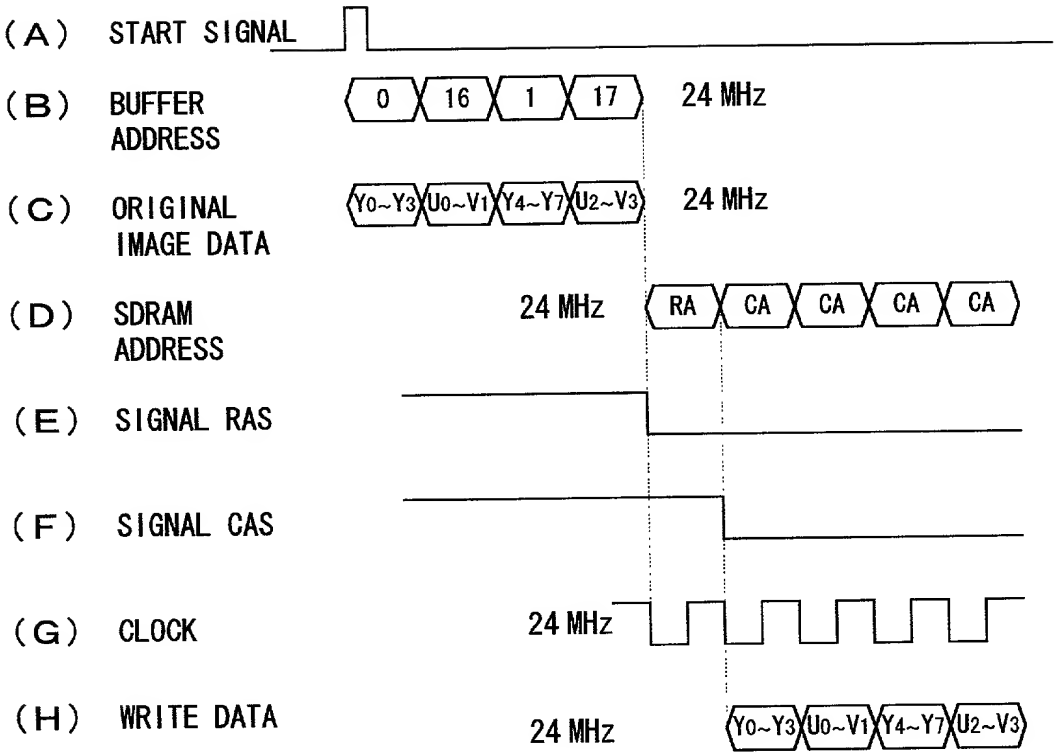

HORIZONTAL
BLANKING PERIOD
(A) Hsync
(B) ORIGINAL
READ
REQUEST
(C) THUMBNAIL
READ
REQUEST
ORIGINAL IMAGE DATA
THUMBNAIL
IMAGE DATA
(D) READOUT
DATA
YC
(E) READOUT
ADDRESS
Y0-Y3
U0-V1
Y4-Y7
U2-V3
Y0-Y24
U0-V12
Y32-Y56
U16-V24
24MH2
24 MHz
0 16 1 17
64 96 65 97

FIG. 8


(A) START SIGNAL
(B) BUFFER ADDRESS
0
16
1
17
24 MHz
(C) ORIGINAL IMAGE DATA
Y0~Y3
U0~V1
Y4~Y7
U2~V3
24 MHz
(D) SDRAM ADDRESS
24 MHz
RA
CA
CA
CA
CA
(E) SIGNAL RAS
(F) SIGNAL CAS
(G) CLOCK
24 MHz
(H) WRITE DATA
24 MHz
Y0~Y3
U0~V1
Y4~Y7
U2~V3

A, W, H, McL & N Docket No._____ ARMSTRONG, WESTERMAN, HATTORI, MCLELAND & NAUGHTON

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **entitled** (Insert Title) DIGITAL CAMERA

the specification of which is attached hereto unless the following is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(List prior foreign applications. See note A on back of this page)				Priority Claimed
Patent Application No. 10-147544	Japan	28 May 1998		☒ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)		
				☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)		
				☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)		
				☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)		

(See note B on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

James E. Armstrong, III, Reg. No. 18,366; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; Le-Nhung McLeland, Reg. No. 31,541; Ronald F. Naughton, Reg. No. 24,616; John R. Pegan, Reg. No. 18,069; William G. Kratz, Jr., Reg. No. 22,631; Albert Tockman, Reg. No. 19,722; Mel R. Quintos, Reg. No. 31,898; Donald W. Hanson, Reg. No. 27,133; Stephen G. Adrian, Reg. No. 32,878; William L. Brooks, Reg. No. 34,129; John F. Carney, Reg. No. 20,276; Edward F. Welsh, Reg. No. 22,455; Patrick D. Muir, Reg. No. 37,403; Gay A. Spahn, Reg. No. 34,978; and John P. Kong, Reg. No. 40,054.

[redacted]

Please direct all communications to the following address:

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Telephone: (202) 659-2930 Fax: (202) 887-0357

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name) Hidefumi OKADA

(See note C above)

Inventor's Signature Hidefumi Okada Date May 7, 1999

Residence Daito-shi, OSAKA, Japan Citizenship Japanese

Post Office Address 5-22-6-205, Fukono, Daito-shi, OSAKA, Japan

Full name of second inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of third inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fourth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fifth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of sixth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of seventh inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of eighth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____